AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0032] with the following amended paragraph:

[0032] Storage controller 102 includes a host interface adapter 202, a storage device interface adapter 206, a microprocessor 204, a bus bridge 208, a buffer memory 212, and a management controller 214. In one embodiment, the host interface adapter 202, storage device interface adapter 206, and microprocessor 204 are each coupled to the bus bridge 208 by a corresponding local bus, as shown. In one embodiment, the local buses comprise a ~~high speed~~ high-speed local bus, including but not limited to a PCI, PCI-X, CompactPCI, or PCI Express bus. In one embodiment, the bus bridge 208 also includes a memory controller for controlling the buffer memory 212. In one embodiment, the buffer 212 and the bus bridge 208 are coupled by a double-data-rate (DDR) memory bus. The bus bridge 208 enables each of the microprocessor 204, host interface adapter 202, and storage device interface adapter 206 to communicate with one another and to transfer data to and from the buffer 212. In one embodiment, the microprocessor 204 comprises a Pentium III® microprocessor, and is coupled to the local bus by a second bus bridge, such as a bus bridge commonly referred to as a north bridge. In one embodiment, the microprocessor 204 is also coupled to a memory for storing program instructions and data for execution by the microprocessor 204. In one embodiment, the management controller 214 comprises an Advanced Micro Devices® Elan™ microcontroller, and is coupled to the local bus by a third bus bridge, such as a bus bridge commonly referred to as a south bridge. In one embodiment, the management controller 214 also is coupled to a memory for storing program instructions and data for execution by the management controller 214.